Rajiv Gandhi University of Knowledge Technologies

T & P Office/Notice/A25/003 Date: 15.07.2024

Job opportunity @ MosChip Technologies

The T&P Team wishes to inform about a job opportunity at MosChip Technologies. MosChip would like to hire B. Tech. ECE &EEE Graduates from class of 2025 to join their team as VLSI Analog Design Intern.

Academic Qualification: 7.25 CGPA in the academics

Compensation Details:

Stipend	: 25K per month (6 Months, Formal Training)
CTC Post Training	: 5.5-6 LPA (12 Months, on job Training)
Service Agreement	: 4.6 Years, Breach amount of 9 Lakhs
Job Location	: Hyderabad
Tentative Joining	: 1st Week of January 2025

Interview Process:

Preliminary Test	: Online (Candidates must be present physically at the campus lab)
Tentative Time of Prelim	: Before end of July 2024
Main exam	: Offline (Students who cleared preliminary test will have to come to the pooled campus post information from our end)
Tentative Time of Mains	: Before end of August 2024
Technical	: Two technical interviews
HR Discussion	: On the same day of main exam

Core Electronics - VLSI Analog Design

MosChip is looking for BE/BTech 2025 batch students with Electronics as a major (ECE, EEE, & EIE) for our requirement in Analog Design Team. Selected students will work on product (ASIC) and IP development, which is a dream job for many core electronics engineers. Students who obtained minimum 65% marks or with 7.25 CGPA are eligible to write the preliminary examination.
Fill in the willing students' information/details in the attached sheet (Excel).

Selection Process:

- Initial screening through online preliminary test for 90 minutes which has questions pooled from Aptitude, Analog and Digital domains
- Followed by the main examination (pen and paper) at the pooled campus which will be of 190 minutes (100 Mins for Analog and 90 Mins for Digital)
- Students who passed/cleared main examination will undergo full day technical evaluation process followed by the HR interview at the pooled campus locations

Analog Design - Job Description:

Candidates will have the opportunity to design various analog design blocks based on the products they work at MosChip. Typically, they would work on the following Blocks:

- Analog-to-digital converters (ADC)
- Digital-to-analog converters (DAC)
- Phase-Locked Loop (PLL), DPLL
- Serializer, De-serializer (Serdes)
- Clock and data recovery (CDR) circuits
- Comparators, Threshold detectors
- Regulators, Power Management Circuits

Key Description:

- Design and development of Analog or Mixed signal macros in cutting edge process technologies; mostly in finfet 5nm/12nm/16nm/28nm/65nm
- Various phases of Analog design; transistor level design, circuit simulation, guiding layout, post layout simulations, parasitic extraction, area optimization, power optimization
- Wreal modelling of the analog blocks
- Electrical characterization on the board in the Lab
- Conceptual level understanding and Architectural level simulations
- Overall SoC concepts of integration, mixed signal simulations, error free designs

How to Apply: If meet the eligibility criteria and interested about this opportunity, please apply through the link https://forms.gle/XG38XRdf8Q4fmBJd8 by July 17, 2024.

Sd/-

T & P Office