Training & Placements/Notice/24-25/163 Date: 04-04-2025

Revolutionize the Future of Computing with Ceremorphic!

Dear Students,

Revolutionize the Future of Computing with Ceremorphic!

We aim to build "Sustainable" Compute Infrastructure – AI semiconductors are the centerpiece of the data-center and enterprise factories of Industry 4.0. Breakthrough evolution of AI model capabilities places stringent and ever-changing demands on performance, cost and power envelope of these AI chips calling for ground up architectures for Intelligent Processing. With more than 200 patents filed Ceremorphic has invented new computing paradigms tailored for the above challenge and is developing silicon and systems products using learnings from decade long research in low power technologies.

Our fast-growing team at Ceremorphic India development center has expertise in Artificial Intelligence hardware and software, digital and analog circuits for multi-terabit processing and communication, device physics, and more. We welcome you to be part of this team developing groundbreaking innovations and shaping the next era of Intelligent Processing with cutting-edge SoC and AI accelerator technologies developed in CMOS nodes from 16nm down to 3nm and beyond! If you are passionate about making a difference and want to be part of a dynamic and innovative team – Ceremorphic is the right place.

About the Role: Engineer – Digital Design

The position involves development of digital subsystems in a complex SoC with multi-core, multi-threaded processor subsystems, AI accelerators, interconnects, memory architecture with multi-level caches, multiple clocks and resets, high-speed interfaces and peripherals. The chosen candidate would do the architecture, microarchitecture and design and verification and would be responsible for the entire design flow and sign-off, including synthesis, LEC, Formality and STA, and be able to deliver reusable and robust digital IP.

Prior Experience

Hands-on experience or Academic Projects involving one or more high end digital designs like multi-core, multi-threaded processor subsystems, high speed interfaces (PCIe, Ethernet, LPDDR, HBM), high performance digital accelerators (Tensor Processing units, Convolution engines, other high performance digital accelerators)

Exposure to design sign-off flows including Lint, CDC, Synthesis, LEC, STA, and Timing Closure.

Familiarity with low-power design methodologies.

Skills Required

Technical Expertise: Verilog, System Verilog, and scripting languages (Python, Perl, Tcl, Shell).

Processor Knowledge: RISC-V, ARM architectures, and protocols like AXI, APB, AHB.

Design Tools: Experience with ASIC and FPGA design flows, DFT (Scan, MBIST, BScan), and UVM methodology.

Analytical Skills: Strong problem-solving abilities with attention to detail.

Low Power Design: Techniques like clock gating, power gating, and dynamic voltage/frequency scaling.

Communication: Good teamwork and collaboration skills, eager to learn and grow.

Educational Requirements: B.Tech or M.Tech/MS in Electronics or Electrical Engineering

Walk-in Interview Details

Dates: April 5, 6, 12, 13, 19, 20

Time Slots:

Please select your preferred timeslot for the interview via the link provided: https://calendly.com/careers-ceremorphic

Location: Ceremorphic Technologies

Interview Process:

The walk-in interview will include a 1-hour written test.

Eligibility Criteria:

Education: B.Tech/BE or M.Tech/MS in Electronics or Electrical Engineering

Aggregate: 70% or above

Experience: 0-2yrs

What to Bring:

An updated resume

A valid Govt. ID for verification

We look forward to meeting you and discussing how you can contribute to our dynamic and innovative team at Ceremorphic Technologies.

Best Regards,

Hiring Team
Ceremorphic Technologies **Best regards,**