RAJIV GANDHI UNIVERSITY OF KNOWLEDGE TECHNOLOGIES-Basar

T&P Office/Notice/22-23/086 **Date: 15.09.2022**

JOB ANNOUNCEMENT OF SMARTSOC SOLUTIONS PVT LTD

It is hereby informed to all Final year(E4) students that the **SMARTSOC SOLUTIONS** would like to conduct recruitment drive for ECE & EEE current final year students. Interested & Eligible students need to register in a given below link by **17th September 2022**

Tentative Schedule of Drive: 23rd September 2022

Link for Registration: http://tnp.rgukt.ac.in

JOB DETAILS & ELIGIBILITY CRITERIA:

Branches: ECE & EEE
CGPA: 7 & Above (throughout Academics) with No Active Backlogs.
Job Designation: Physical Design Engineer, RTL Design Engineer, Design Verification Engineer, Analog Layout Engineer.
Job Location: Bangalore/Hyderabad/Chennai/Hubli**.**
Agreement: 3 Years (Breakage Amount: 6 Lakhs).
CTC: 6 LPA
Internship: Yes
Internship Stipend: 10000/-PM

EMPLOYMENT CONDITIONS:

1. **Contract Duration:** 3 Years for both B.Tech.
2. **Contract Cancellation:** If the selected candidates are breaking the contract or leaving the company before the completion of the contract period, then the candidate has to repay the training cost informed by the company.

DETAILED INFORMATION ON HIRING POSITIONS:

1. **Physical Design Engineer:** As a Physical Design and Implementation Engineer, you will develop high performance hardware and software to enable Google's continuous innovations in working with Application Specific Integrated Circuits (ASIC). You will work with Architects and Logic Designers to drive architectural feasibility studies, develop timing, power, and area design goals and explore Register Transfer Language (RTL)/design trade-offs for physical design closure.
2. **RTL Design Engineer:** As a RTL Design Engineer, you will oversee definition, design, verification, and documentation for SoC (System on a Chip) development. You will be involved in SoC/Sub-System microarchitecture definition, IP/Sub-System design, system simulation/debug and IP integration.
3. **Design Verification Engineer:** As a Design Verification Engineer you will be Responsible for verification of the ASIC design, architecture, golden models and micro-architecture of PCIE controllers at IP/sub-system levels using state-of-the-art verification methodologies such as UVM. You are expected to understand the design specification and implementation, define the verification scope, develop test plans, tests, and the verification infrastructure and verify the correctness of the design. You will be collaborating with architects, designers, and pre and post silicon verification teams to accomplish your tasks.
4. **Analog Layout Engineer:** As a member of the AMS layout team you will be responsible to deliver a fully-verified, clean layout, this includes the following: Designing complex layout for mixed signal, and analog circuits in deep sub-micron CMOS technologies. Reviewing and analyzing floor plans and complex circuits with circuit designers

Note: As per policy by SmartSoc, if any Student receives an offer those students are not allowed for next placement drives.

Sd/-
Placement Office