Rajiv Gandhi University of Knowledge Technologies

T & P Office/Notice/A24/011 Date: August 29, 2023

Job Announcement of MosChip Technologies

T&P is to inform E4 students about a career opportunity at **MosChip Technologies**. MosChip is looking for BE/BTech 2024 batch students with **Electronics as a major stream** (ECE & EEE) for their requirement in Analog Design Team. Selected students will work on product (ASIC) and IP development, which is a dream job for many core electronics engineers.

Job Details and Eligibility

Academic Qualification: Above 65%/7.25 CGPA in the academics

Compensation Details

Stipend	: **25K** per month (6 Months, Formal Training)
CTC Post Training	: **5.5-6 LPA** (12 Months, On job Training)
Service Agreement	: **4.6 Years**, Breach amount of **9 Lakhs**
Job Location	: Hyderabad
Tentative Joining	: 18th December (Tentatively)

Selection Process:

- Preliminary test which will be online of 90 minutes
- Followed by the main exam (pen and paper) at the pooled campus, which will be 120 minutes. (We have pooled campus finalized like Hyderabad, Vizag, Guntur, Kakinada, Vizianagaram, Anantapur tentatively)
- Main exam cleared students will undergo two technical interviews followed by the HR interview at the pooled campus locations.

Analog Design - Job Description:

Candidates will have the opportunity to design various analog design blocks based on the products they work at MosChip. Typically, they would work on the following Blocks:

- Analog-to-digital converters (ADC)

- Digital-to-analog converters (DAC)
- Phase-Locked Loop (PLL), DPLL
- Serializer, De-serializer (Serdes)
- Clock and data recovery (CDR) circuits
- Comparators, Threshold detectors
- Regulators, Power Management Circuits

They may also work on designing general-purpose high-performance CMOS circuits like the following:

- Bandgap reference
- Bias circuits
- Switching circuits
- Amplifiers
- Oscillators

Key Description:

- Design and development of Analog or Mixed signal macros in cutting edge process technologies; mostly in finfet 5nm/12nm/16nm/28nm/65nm
- Various phases of Analog design; transistor level design, circuit simulation, guiding layout, post layout simulations, parasitic extraction, area optimization, power optimization
- Wreal modelling of the analog blocks
- Electrical characterization on the board in the Lab
- Conceptual level understanding and Architectural level simulations
- Overall SoC concepts of integration, mixed signal simulations, error free designs

How to Apply: If meet the eligibility criteria and interested about this opportunity, please apply through the Training & Placement Portal (https://tpcrt.rf.gd) by **30 August 2023.**

Sd/-
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