Rajiv Gandhi University of Knowledge Technologies

(Telangana Government Act 8 of 2016)

Basar, Nirmal, Telangana State – 504107, India.

A.Y 25-26_E3_SEM1_ELECTRONICS AND COMMUNICATION ENGINEERING TIME TABLE

Year	Time	Mon	Tue	Wed	Thu	Fri	Sat
C1(ECE Seminar hall)	Slot-1	A	A	E	G	A	
	Slot-2	C	C	D	A	D	
	Slot-3	F	D	C	D	E	
	LUNCH BREAK						
	Slot-4	Y(B1)	B	F	E	B	
	Slot-5		G	Z(B1&B2)	B	Y(B2)	
	Slot-6						

Year	Time	Mon	Tue	Wed	Thu	Fri	Sat
C2(ECE-F25)	Slot-1	E	G	D	A	D	
	Slot-2	B	D	C	D	Y(B2)	
	Slot-3	C	C	A	E		
	LUNCH BREAK						
	Slot-4	A	Y(B1)	E	F	F	
	Slot-5	G		B	Z(B1&B2)	B	
	Slot-6			A			

Year	Time	Mon	Tue	Wed	Thu	Fri	Sat
C3(ECE-G12)	Slot-1	D	E	E	D	E	
	Slot-2	A	D	D	Y(B2)	C	
	Slot-3	B	C	F		A	
	LUNCH BREAK						
	Slot-4	C	A	A	B	G	
	Slot-5	Z(B1&B2)	B	Y(B1)	G	F	
	Slot-6						

Year	Time	Mon	Tue	Wed	Thu	Fri	Sat
C4(ECE-G22)	Slot-1	C	D	D	E	C	
	Slot-2	D	C	Y(B2)	D	A	
	Slot-3	E	G		A	B	
	LUNCH BREAK						
	Slot-4	B	F	B	Y(B1)	E	
	Slot-5	A	Z(B1&B2)	A		G	
	Slot-6	F					

	Time
Slot-1	09:00 AM to 09:55 AM
Slot-2	10:00 AM to 10:55 AM
Slot-3	11:00 AM to 11:55 AM
LUNCH BREAK	
Slot-4	1.30 PM to 2.25 PM
Slot-5	2.30 PM to 3:25 PM
Slot-6	3.30 PM to 4.25 PM

	Course code	Course Name	L-T-P	TOTAL CONTACT HOURS	FACULTY
A	EC3101	Analog and Digital Communications	3-1-0	4	Mr.B.Adhithya(C1,C2,C3,C4)
Y	EC3701	Analog and Digital Communications lab	0-0-2	2	Mr.K .Karthik(C1(B1),C2(B1),C3(B1),C4(B1)), Mrs.Gayathri(C1(B2),C3(B2),C4(B2)),Mr.K.Anjani Kumar((C2(B2))
B	EC3102	Computer Architecture	3-0-0	3	Mrs.B.Neelima (C1,C2,C3,C4)
C	EC3103	Digital Signal Processing	3-0-0	3	Dr.G.V S S K R Naganjaneyulu(C1,C2),Mrs.Gayathri(C3,C4)
Z	EC3702	Digital Signal Processing lab	0-0-2	2	Mr.G.Srinivs Sagar(C1(B1),C2(B1),C3(B1),C4(B1)) ,Mr.A.Dheeraj (C1(B2),C4(B2)) Mrs.Gayathri(C2(B2),C3(B2))
D	EC3104	VLSI Engineering	3-1-0	4	Mr.A.Sainath Chaitanya (C1,C2) Mr.R.Saidulu (C3,C4).
E	BM3107	Managerial Economics and Financial analysis	3-0-0	3	Sandya Rani(C1),Mrs.B.Srividya(C2,C3,C4)
F	HS31XX	Corporate Communications	0-0-2	2	Dr.N.Vijay Kumar(C1,C2,C3),Chadrashekar(C4)
G		Data Structures	3-0-0	3	Mr.Thilok Reddy(C1,C2,C3,C4)

(Mr.R.Saidulu)
Faculty I/c, Dept. Timetables

(Mr.B.UpendeRao)
(HOD/ECE)

(Mr.K.Mahesh)
Associate Dean Engineering