



Ceremorphic – Campus Recruitment -2027

Ceremorphic has invited applications from eligible **B.Tech students of RGUKT-Basar** for the position of **Software – AI / ML, Digital Design & Analog Custom Design Engineer** at Hyderabad.

Location: Hyderabad

CTC: ₹13.5 LPA

Eligible Branches: CSE & ECE

Internship: 12 months

- First 6 months: ₹30,000/month stipend
 - Next 6 months: ₹40,000/month stipend
- Bond/Service Contract:** Applicable as per company terms

Roles & Key Skill Requirements

1. Software – AI / ML

Deep Learning Infrastructure Engineer

As a Deep Learning Infrastructure Engineer, you will play a crucial role in bridging the gap between deep learning software and custom hardware accelerators. The role demands a strong foundation in C/C++ programming, experience working in a Linux environment, proficiency with Git workflow, and strong Python programming skills. The ability to work independently and a good understanding of both software and hardware aspects of deep learning are essential.

While experience with deep learning compilers and OpenCL programming is good to have, proficiency in deep learning models, algorithms, and high-performance algorithm design is crucial. Additionally, familiarity with machine learning frameworks, deep learning model architectures, and hardware accelerators can significantly enhance your effectiveness in this position.

Responsibilities

- **Tool Development:** Create and enhance tools for compiling deep learning models optimized for Ceremorphic chips.
- **Collaboration:** Work with deep learning software framework teams and hardware architecture teams to enhance deep learning software.
- **API Definition:** Define public APIs to facilitate interactions between software and hardware.
- **Performance Tuning:** Analyse and optimize the performance of compiled models.
- **General Software Engineering:** Engage in various software engineering tasks to support the development lifecycle.

Key Requirements

- **C/C++ Programming:** Proficiency in C/C++ for software design, debugging, performance analysis, and test design.

- **Linux Environment:** Experience working in a Linux environment.
- **Git Workflow:** Proficiency with Git workflow for version control.
- **Python Programming:** Strong skills in Python programming.
- **Independent Work:** Ability to independently define project goals and scope, and lead development efforts.
- **Technology Proficiency:** Experience with deep learning models, algorithms, framework design, and high-performance algorithm design.

Good to Have Skills

- **Machine Learning Frameworks:** Experience with high-level frameworks such as TensorFlow, PyTorch, and MXNet.
- **Network Architectures:** Familiarity with popular neural network architectures like Mistral, Mixtral, Llama, ResNet, MobileNet, and SSD.
- **Hardware Accelerator Knowledge:** Understanding of machine learning hardware accelerators, including their architectures and common techniques.
- **Deep Learning Compiler Experience:** Experience with compilers like MLIR, ONNC, TVM, and XLA.

2. Digital Design

About the Role

Looking for candidates to work on digital design of **high-performance and low-power Microprocessor / Machine Learning Processor / Logic Designs**.

Key Requirements

- Any project experience having hands-on experience in **microarchitecture and logic design**, along with RTL coding for the same.
- Strong **Digital Design Fundamentals**.
- Project experience should preferably be **from scratch**, along with the adequate hardware knowledge required for realizing those projects.
- Good **Verilog coding skills**.
- Preferred knowledge in **RISC-V architectures and pipelined processors**.
- Preferred experience in **signoff flows**, including:
 - Lint
 - CDC
 - Synthesis
 - STA timing closure
- Any true research potential demonstrated through **truly self-developed new ideas or innovations** would be a genuine advantage.
- Any knowledge of **true-from-scratch GPT/AI/ML** is a bonus.

Preferred Skills

- Curious Explorer and Continuous Learner
- Problem Solver, Critical Thinker & Quick Learner
- Responsible and Accountable Owner
- A Humble Team Player

3. Analog Custom Design:

A key component of our system is the high-speed interconnect. The Designer would be in charge of a core part of the high-speed PHY, including PCIe, Ethernet, and USB, in advanced FinFet technology nodes. A strong understanding of analog/mixed-signal circuit theories, and expert hands-on design skills, are keys to a successful candidate for this position.

Key requirements:

- Basic understanding of high-speed interface concepts such as PLLs, CDRs, serializers/deserializers, transmitters, receivers, or related communication systems through coursework, projects, or internships.
- Familiarity with CMOS circuit design and simulation using industry-standard EDA tools, including schematic entry, simulation, and waveform analysis.
- Understanding of circuit trade-offs involving power, performance, area, speed, and reliability.
- Exposure to physical layout concepts, including matching techniques, common-centroid layout, device symmetry, parasitic effects, and basic verification flows.
- Experience through academic projects, internships, or research work related to analog, mixed-signal, RF, VLSI, or communication systems is preferred.
- Strong analytical and problem-solving skills with the ability to learn new concepts and technologies quickly.
- Good communication skills and the ability to present technical work clearly and collaborate effectively within a team environment.
- Enthusiasm to work on advanced semiconductor technologies and contribute to the development of next-generation high-speed interconnect solutions.

Additional Skills:

Exposure to FinFET technologies, high-speed PHY architectures, PCIe, Ethernet, USB, or PAM4 signaling is an added advantage but not mandatory.

Important Instructions

- Students should register only for roles matching their **branch, technical skills, projects and area of interest**.
- The recruitment includes a **12-month internship-cum-job opportunity**, subject to company requirements and applicable terms.
- Students should be prepared to discuss their academic/technical projects in detail during the technical interviews.
- Registration does not guarantee shortlisting or selection. Final selection will be at the sole discretion of the company.

Registration Link: <https://forms.gle/xnNdmoJ4n8ayMjDE6>

Last Date & Time for Registration: **08.10.2026, 4:00 PM.**

Training & Placement Office

RGUKT-Basar