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RGUKT/Acad/NB-Hub/2026-27 **Date:16.08.2026**

CIRCULAR

Sub: Registration for VLSI Design Boot Camp for ECE and EEE Students and Faculty – Reg.

As per the MoU with NIELIT, a VLSI Design Boot Camp is scheduled to be conducted from 18.08.2026 to 22.08.2026 for the Departments of ECE and EEE.

Faculty members and students of E2 to E4 from the ECE and EEE departments are eligible to register for the boot camp. The boot camp covers key areas of Verilog, RTL design, synthesis, IP design, bus interfaces, clock-domain crossing (CDC), clocking, low-power design, and SoC integration.

The detailed schedule of the boot camp is attached for your kind reference.

A certificate will be issued to all registered participants who successfully clear the examination conducted as part of the boot camp.

All eligible students and faculty members are encouraged to register and actively participate in the programme.

The registration will be conducted through spot registration on 18.08.2026, from 9:30 AM to 11:30 AM.

The inauguration of the boot camp will be held at 11:30 AM on 18.08.2026 at the AB3 Conference Hall.

-sd/-

Dr. K. Mahesh

Associate Dean Engineering

RAJIV GANDHI UNIVERSITY OF KNOWLEDGE TECHNOLOGIES
Basar

इलेक्ट्रॉनिकी एवं सूचना प्रौद्योगिकी मंत्रालय
MINISTRY OF ELECTRONICS AND INFORMATION TECHNOLOGY
सत्यमेव जयते Government of India

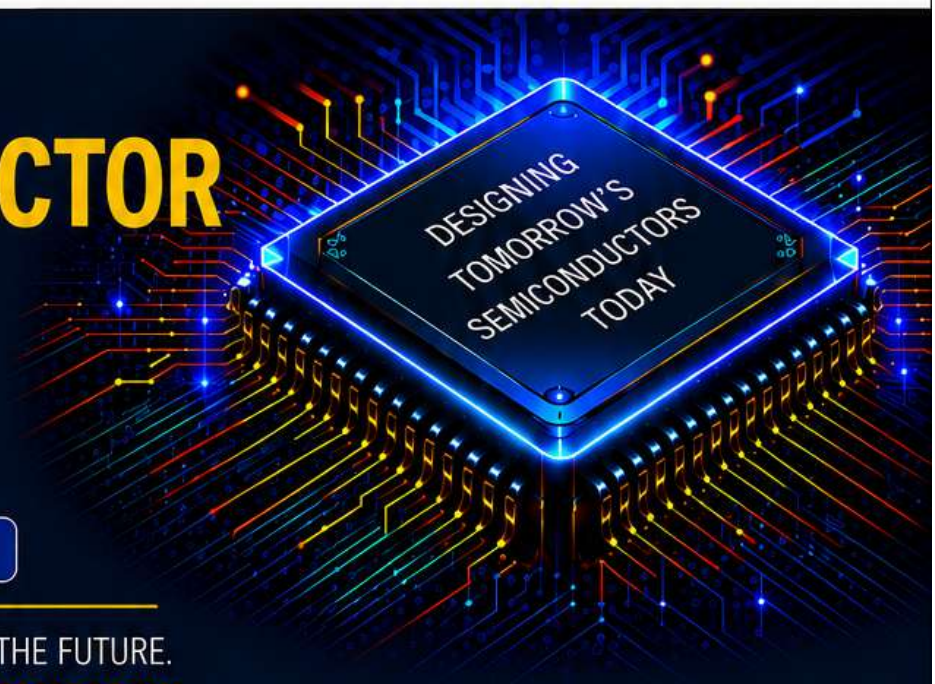
NIELIT HYDERABAD

5-DAY BOOTCAMP ON

SEMICONDUCTOR DESIGN:

RTL, IP INTEGRATION, AND SOC SIGNOFF

Using Open-Source EDA Tools



A HANDS-ON BOOTCAMP TO DESIGN THE FUTURE.
BUILD SEMICONDUCTORS. BUILD TOMORROW.

COMMENCES FROM 18TH – 22ND AUGUST 2026

DURATION 5 DAYS

HANDS-ON PRACTICE

CERTIFICATE TO SUCCESSFUL CANDIDATES

COURSE FEE NIL 100% FREE

WHAT YOU WILL LEARN – HANDS-ON PRACTICE ON

- RTL Design & Coding (SystemVerilog)
- Functional Verification
- Synthesis using Open Source Tools
- IP Integration
- SoC Signoff (DFT, STA, Lint)
- From Concept to Silicon – Your Design Journey

COURSE HIGHLIGHTS

- Hands on Practice on RTL design and Coding
- Functional Verification
- Synthesis using Open Source Tools
- IP Integration & SoC Signoff
- Learn Industry-Relevant Semiconductor Design Skills
- Guidance from Experts

WHO CAN ATTEND?

- B.Tech & M.Tech (undergoing or completed) of ECE & EEE
- Faculty members
- Working professionals in chip design

YOU WILL GAIN

- Industry-standard skills in semiconductor design
- Hands-on experience with open-source tools
- Practical exposure to real-world design flow
- Certificate of completion (after clearing the exam)

- Learn Industry-Relevant Semiconductor Design Skills
- Hands-On with Industry-Standard Tools & Flows
- Learn from Experts & Industry Practitioners
- Enhance Your Career Prospects in the Semiconductor Industry
- Certificate of Completion

NO FEE. JUST LEARNING. LIMITED SEATS!

Bootcamp for the MeitY funded project on

EdTech Platform in Semiconductor Space to Democratize Chip Design and Development Ecosystem for Masses

Day wise plan of the bootcamp

Day	Focus area	Topics to be covered
Day 1 **Verilog Fundamentals & Tool Flow**	RTL Basics + Linux	• Fundamentals of Verilog: syntax, modules, hierarchy • Behavioural vs Structural modelling • Linux & VI command lab **Hands-on Labs:** • AND gate in Verilog • 4-bit counter • Ripple up counter • Verilator: 4×1 MUX • Verilator: Half Adder
Day 2 **Synthesis & IP Design Basics**	Synthesizable RTL + IP Flow	• Synthesizable vs Non-synthesizable constructs • Common RTL coding mistakes • Introduction to Yosys (RTL → Gate) • Synth vs Non-synth examples (practical comparison) **Hands-on Labs:** • JK Flip-Flop (synth-safe RTL) • Synth vs non-synth RTL demo • IP design methodology: Specification → RTL → Verification • UART RX (simple RTL)
Day 3 **Bus Interfaces, CDC & Clocking**	IP Integration+ Timing	• IP integration at subsystem level • Signal interfacing basics • Bus protocols overview (APB focus) • APB-UART integration

		CDC & Reset Concepts: • Metastability (without synchronizer) • Fixing metastability using 2-stage synchronizer • CDC & RDC handling basics • Introduction to SoC clocking & reset architectures • Reset types (sync/async)
Day 4 **Low Power, Multi-Clock & Reset Design**	Advanced RTL Techniques	• Multi-clock domain architectures • Clock multiplexers & dividers • Multi-stage synchronizers for stable CDC • FIFO design for asynchronous interfaces **Low Power Design:** • Clock gating concepts & RTL coding • Power gating introduction • UPF low-power basics • Low-power Verilog coding exercises • Reset architecture: global & local resets • Reset synchronization logic
Day 5 **Mini-SoC Project & Debugging**	Integration + Industry Practice	• Designing simple IPs: UART, GPIO, Timer • Writing bus interfaces (APB / AHB-Lite basics) • Inserting clock/reset synchronization logic • Integrating multiple IPs into a mini-SoC **Project & Collaboration:** • Mini-SoC project using GitHub • Team-based collaboration using GIT • Debugging SoC integration – detecting a real bug • Introduction to assertions for CDC/RDC checking