

Rajiv Gandhi University of Knowledge Technologies

(A.P. Govt. Act 18 of 2008 & Telangana Govt. Adaptation G.O. Ms No.29 Dt.17.12.2014) Basar (Village & Mandal), Nirmal District, Telangana State – 504107, India.

Date: 12.12.2020

Webpage: www.rgukt.ac.in Training & Placement Office

RGUIIIT-Basar/Placement/Notice Board/20-21/081

JOB DESCRIPTION OF EFFTRONICS DRIVE

Eligibility Criteria:- 70% and Above with no backlogs

They have requirement for below positions:

Embedded Engineer - B. E. / B. Tech. (ECE, EIE) Software Engineer - B. E. / B. Tech. (CSE,IT, MCA)

GROUP NAME:

- (i) RGUKT BASAR @ FIRMWARE ENGINEER [ECE-EIE]-2021
- (ii) RGUKT BASAR @ SOFTWARE ENGINEER [CSE-IT- MCA]-2021

SELECTION PROCESS:

- Written Test
- Technical Interview
- · Technical Final round
- HR Interview
- Fitness Test

TERMS & CONDITIONS:

- 1. There would be **2.5 years'** agreement with the company wherein the Candidate needs to submit all his/her original Certificates for the agreement period.
- 2. Training period would be for a total period of 6 months.

IMPORTANT LINKS & DATES:

- **Online link for Registration URL: http://efftronics.runexam.com/register.aspx
- **Online Exam scheduled on 16-Dec -20 at 11:30 AM.
- **Examination link: https://candidate.speedexam.net/signin.aspx?site=efftronics (To be sign with registered user ID and Password on the exam day.
- **We will have Pre placement talk virtually on **16-Dec -20 at 10:15 AM 11:15 AM** (Pre Placement Talk Link will be shared a day before).

^{***}Please go through the below JD's.

Position Brief:

Designation: Software Engineer Trainee

Location of Posting: Vijayawada **Package:** 3.5 - 8.5 Lac CTC per annum

The following areas will be tested during the selection procedure:

S. No	Topics
1	Combinations Logic Circuits
2	Sequential Logic Circuits
3	Software Programming
4	Protocols
5	Algorithms
6	Oops Concepts
7	Computer Organization & Architecture
8	DBMS
9	Physics
10	Mathematics
11	Aptitude

Designation: Embedded Trainee Location of Posting: Vijayawada **Package:** 3.5 - 8.5 Lac CTC per annum

The following areas will be tested during the selection procedure:

S. No	Topics
1	Combinations Logic Circuits
2	Sequential Logic Circuits
3	Software Programming
4	Protocols
5	Algorithms
6	Circuit Theory(EDC)
7	Basic Electronics
8	Micro Processor & Micro Controllers
9	Physics
10	Mathematics
11	Aptitude